AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (cancelled)

Claim 2 (cancelled)

Claim 3 (previously presented) A stacked-gate flash memory cell having a floating Poly-Si gate with multiply connected surfaces of individual shapes comprising:

a semiconductor substrate having an active area;

a floating Poly-Si gate with a bottom surface and a multiply connected top surface;

said bottom surface being flat and overlying said active area;

said multiply connected top surface overlying said bottom surface; said multiply connected top surface being defined by multiple regions of individual cross-sectional shapes, wherein the area of said multiply connected top surface overlying said active area is greater than the area of said bottom surface;

wherein said individual cross-sectional shapes are selected from a group consisting of rectangular, trapezoidal and triangular shapes;

a conformal inter-poly dielectric layer replicating said individual cross-sectional shapes over said floating Poly-Si gate; and

a conformal Poly-Si control gate replicating said individual cross-sectional shapes over said inter-poly dielectric layer;

wherein said regions of individual cross-sectional shapes have a depth between about 900 to 1000Å.

Claim 4 (cancelled)

Claim 5 (currently amended) ~~A~~ The stacked-gate flash memory cell of claim ~~1~~3, wherein said inter-poly dielectric layer is oxide-nitride-oxide having a thickness between about 150 to 250Å.

Claim 6 (currently amended): ~~A~~ The stacked-gate flash memory cell of claim ~~1~~3, wherein said Poly-Si control gate has a thickness between about 1500Å to 2000Å.

Claims 7-20 (cancelled)

Claim 21 (new): The stacked-gate flash memory cell of claim 3, wherein said floating Poly-Si gate has a thickness between about 1900Å to 2100Å.